


LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
-	Original release	04-12-10	B. LaBelle
A	Updated Table II, expanded section 4.0 (Tables III – VI), added section 5.0 (Table VII), corrected various Figures	09-03-10	B. LaBelle
B	Corrected subgroups and values in Table II, deleted subgroups 5 and 6 for Final & Group A and added Post Seal electrical in table IV; corrected typo for temp testing and added Post Seal electrical in Table III	09-16-10	B. LaBelle
C	Remove Non-Destructive Wire Pull as a Standard Screening process for Space Applications, revised Static Burn-in Condition and corrected typos.	01-12-11	B. LaBelle
D	Corrected case outline designator on sheet 2 from F to X	02-09-11	B. LaBelle
E	Revise and update to QCI Lot Quantities per MS 883 Method 5005.15 Tables IIa, IIb, IV	08-30-11	B. LaBelle
F	Replace case outline on page 9	11-15-11	B. LaBelle

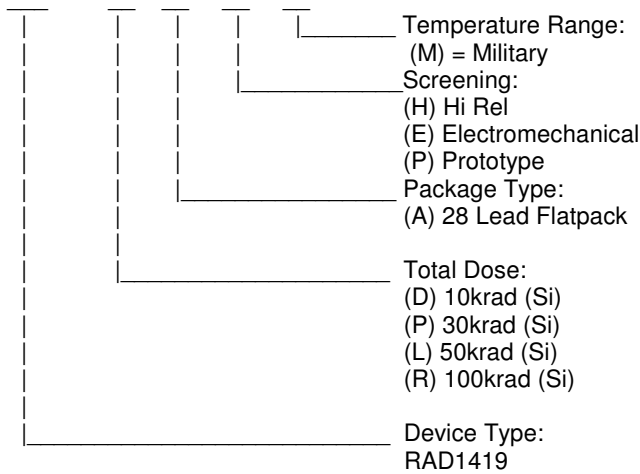
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<p>UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON DECIMALS XX=+-.03 XXX=+-.010</p>	<p>PREPARED BY T. Evans</p>				
	<p>CHECKED BY S. Love</p>				
	<p>Aeroflex RAD, Inc.</p>	<p>APPROVED BY R. LaBelle</p>	<p>SPECIFICATION FOR Microcircuit, Analog to Digital Converter, 14 Bit Sampling, Low Power, RAD1419</p>		
		<p>DRAWING APPROVAL DATE 04-12-10</p>			
<p>Product Specification</p>	<p>REVISION LEVEL Rev F</p>	<p>SIZE A</p>	<p>CAGE CODE 3KTA5</p>	<p>DRAWING NUMBER RAD-1419ADC-01</p>	
	<p>UNCONTROLLED COPY</p>	<p>SHEET 1 OF 19</p>			

1. **SCOPE:** This drawing documents high reliability requirements for space application (device class V). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.1 **PIN.** The PIN (Part Identification Number) is as shown in the following example:

RAD1419 - * * * *



Notes:

Military temperature range is -55° to 125 °C.

Prototype tested at 25 °C, no screening.

Electromechanical is a 3 temperature test at 25 °C, -55 °C, and 125 °C, no screening.

1.2 **RHA designator.** Device classes Q and V equivalent devices are compliant to the MIL-PRF-38535 specified RHA levels (D,P,L,R) and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.3 **Device type(s).** The device type(s) identify the circuit function as follows:

<u>Generic number</u>	<u>Circuit function</u>
1419A	14 bit A to D Converter

1.4 **Device class designator.** The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
H	Level V Equivalent with MIL-PRF-38535
E	Electro-Mechanical
P	Prototype

1.5 **Case outline(s).** The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
A	CDFP4-F28	28	Flat Package

1.6 **Lead finish.** The lead finish is as specified in MIL-PRF-38535 for device classes V or MIL-PRF-38535.

1.7 **Absolute maximum ratings.** Table I

AVDD = VDD = DVDD (Notes 1,2)	
Supply Voltage (VDD).....	6V
Negative Supply Voltage (VSS).....	-6V
Total Supply Voltage (VDD to VSS).....	12V
Analog Input Voltage (Note 3).....	(VSS - 0.3V) to (VDD + 0.3V)

Product Specification	SIZE A	CAGE CODE 3KTA5	DRAWING NUMBER RAD-1419ADC-01
	Aeroflex RAD, Inc. Proprietary UNCONTROLLED COPY	REVISION LEVEL F	SHEET 2 of 19

Digital Input Voltage (Note 4).....(VSS - 0.3V) to 10V
 Digital Output Voltage.....(VSS - 0.3V) to (VDD + 0.3V)
 Power Dissipation.....500mW
 Operating Temperature Range.....-55 °C to +125 °C
 Storage Temperature Range-65 °C to +150 °C
 Lead Temperature (soldering, 10s)+300 °C

See Notes at the end of Table II

1.8 Radiation features: Maximum total dose available (MIL-STD-1017 Condition A)

- D, 10krad(Si)
- P, 30krad(Si)
- L, 50krad(Si)
- R, 100krad(Si)

2. APPLICABLE DOCUMENTS

- 2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.
- 2.1.1 DEPARTMENT OF DEFENSE SPECIFICATION - MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.
 - 2.1.2 DEPARTMENT OF DEFENSE STANDARDS
 - 2.2.1.1 MIL-STD-883 -Test Method Standard Microcircuits.
 - 2.2.1.2 MIL-STD-1835 -Interface Standard Electronic Component Case Outlines.
 - 2.1.3 DEPARTMENT OF DEFENSE HANDBOOKS
 - 2.1.3.1 MIL-HDBK-103 - List of Source Control Drawings.
 - 2.1.3.2 MIL-HDBK-780 - Source Control Drawings.
 - 2.1.4 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

2. REQUIREMENTS

- 3.1 Item requirements. The individual item requirements for Hi-Rel device shall be in accordance with MIL-PRF-38535 class V and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.
- 3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device class V.
 - 3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.
 - 3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.
 - 3.2.3 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 3.
 - 3.2.4 Typical Performance Characteristics Figure 4.
 - 3.2.5 Burn-in circuit. The burn-in circuit shall be as specified on figure 5.
 - 3.2.6 Life test circuit. The life test circuit shall be as specified on figure 5.
 - 3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 6.
- 3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in 1.3 - Table I and shall apply over the full case operating temperature range.
- 3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in Table II.
- 3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein, date code and manufacture name or Logo. A unique serial number will be marked on the back of the package.
- 3.6 Certificate of Conformance. A certificate of conformance to the requirements of this drawing will be provided with each lot of microcircuits delivered to this drawing.
- 3.7 Radiation Certificate. A radiation certificate of conformance shall be provided with each lot reporting the radiation test results from wafer lot qualification testing per paragraph 5.0 herein. The certificate guarantees the radiation performance as outlined in this specification.

TABLE II. Electrical performance characteristics.

Product Specification	SIZE A	CAGE CODE 3KTA5	DRAWING NUMBER RAD-1419ADC-01
	Aeroflex RAD, Inc. Proprietary UNCONTROLLED COPY	REVISION LEVEL F	SHEET 3 of 19

CONVERTER CHARACTERISTICS * denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C. With Internal Reference (Notes 5,6)

PARAMETER	SYM	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
Resolution		(No Missing Codes)	1	14			Bits
			2				
			3				
Integral Linearity Error	INL	Note 7/	1		±0.8	±2	LSB
			2				
			3				
Differential Linearity Error	DNL		1		±0.7	±1.5	LSB
			2		±0.7		LSB
			3		±2	LSB	
Offset Error		Note 8/	1		±5	±20	LSB
			2				
			3				
Full scale Error Internal Reference			1		±10	±60	LSB
Full scale Error External Reference		2.5V			±5		LSB
Full Scale Tempco		IOUT(REF) = 0			±15		ppm/°C

ANALOG INPUT (* denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C.) Note 5

PARAMETER	SYM	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
Analog Input Range	VIN	Note 9/, $4.75V \leq VDD \leq 5.25V$, $-5.25V \leq VSS \leq -4.75V$ *			±2.5		V
Analog Input Leakage Current	IIN	CS\ = HIGH	1			±1	µA
			2				
			3				
Analog Input Capacitance	CIN	Between Conversions			15		pF
Analog Input Capacitance	CIN	During Conversions			5		pF
Sample-and-Hold Acquisition Time	tACQ	Note 9/			90	300	ns
Sample-and-Hold Aperture Delay Time	tAP				-1.5		ns
Sample-and-Hold Aperture Delay Time Jitter	tjitter				2		psRMS
Analog Input Common Mode Rejection Ratio	CMRR	$-2.5V < (-AIN = AIN) < 2.5V$			60		dB

Product Specification

Aeroflex RAD, Inc. Proprietary
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SIZE
A

CAGE CODE
3KTA5

REVISION LEVEL
F

DRAWING NUMBER
RAD-1419ADC-01

SHEET
4 of 19

TABLE II. Electrical performance characteristics (continued)

DYNAMIC ACCURACY (* denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C.) Note 5

PARAMETER	SYM	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
Signal-to(Noise + Distortion) Ratio	S/(N + D)	100kHz Input Signal *	4	78	81.5		dB
Signal-to(Noise + Distortion) Ratio	S/(N + D)	390 kHz Input Signal *	4		80.0		dB
Total Harmonic Distortion	THD	100kHz Input Signal, First 5 Harmonics *	4		-93	-86	dB
Total Harmonic Distortion	THD	390 kHz Input Signal, First 5 Harmonics *	4		-86		dB
Spurious Free Dynamic Range	SFDR	100KHz Input Signal *	4		-95	-86	dB
Intermodulation Distortion	IMD	fIN1 = 29.37kHz, fIN2 = 32.446kHz	4		-86		dB
Full-Power Bandwidth					20		MHz
Full-Linear Bandwidth		S/(N + D) ≥ 77dB			1		MHz

INTERNAL REFERENCE CHARACTERISTICS Note 5

PARAMETER	SYM	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
Output Voltage	VREF	IOUT = 0	1	2.480	2.500	2.520	V
			2				
			3				
Output Tempco	VREF	IOUT = 0			±15		ppm/°C
Line Regulation	VREF	4.75V < VDD < 5.25V, -5.25V < VSS < -4.75V			0.05		LSB/V
Output Resistance	VREF	-0.1mA < IOUT < 0.1mA			2		kΩ
Output Voltage	REF comp	IOUT = 0			4.06		V

DIGITAL INPUTS AND DIGITAL OUTPUTS (* denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C.) Note 5

TEST	SYM	TEST CONDITION	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
High Level Input Voltage	VIH	VDD = 5.25V * Note 12	1	2.4			V
			2				
			3				
Low Level Input Voltage	VIL	VDD = 4.75V * Note 12	1			0.8	V
			2				
			3				
Digital Input Current	IIN	VIN = 0V to VDD *	1			±10	μA
			2				
			3				

Product Specification

Aeroflex RAD, Inc. Proprietary
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SIZE
A

CAGE CODE
3KTA5

REVISION LEVEL
F

DRAWING NUMBER
RAD-1419ADC-01

SHEET
5 of 19

TEST	SYM	TEST CONDITION	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS	
Digital Input Capacitance	CIN	Note 9/			5		pF	
High Level Output Voltage	VOH	VDD = 4.75V IO = -10µA*			4.5		V	
High Level Output Voltage	VOH	VDD = 4.75V IO = -200µA	1	4.0			V	
			2					
			3					
Low Level Output Voltage	VOL	VDD = 4.75V IO = 160µA			0.05		V	
Low Level Output Voltage	VOL	VDD = 4.75V IO = 1.6mA *	1			0.10	0.4	V
			2					
			3					
High-Z Output Leakage D13 to D0	IOZ	VOUT = 0V to VDD, CS\ High *	1				±10	µA
			2					
			3					
High-Z Output Capacitance D13 to D0	COZ	CS\ High, Note 9/ *				15	pF	
Output Source Current	ISOURCE	VOUT = 0V			-10		mA	
Output Sink Current	ISINK	VOUT = VDD			10		mA	

POWER REQUIREMENTS (* denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C.) Note 5

PARAMETER	SYM	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
Positive Supply Voltage	VDD	Note 10/		4.75		5.25	V
Negative Supply Voltage	VSS	Note 10/		-4.75		-5.25	V
Positive Supply Current	IDD		1		11	20	mA
			2				
			3				
Positive Supply Current	IDD	Nap Mode: SHDN\ = 0V, CS\ = 0V			1.5		mA
Positive Supply Current	IDD	Sleep Mode: SHDN\ = 0V, CS\ = 5V			250		µA
Negative Supply Current	ISS		1		19	30	mA
			2				
			3				
Negative Supply Current	ISS	Nap Mode: SHDN\ = 0V, CS\ = 0V			100		µA
Negative Supply Current	ISS	Sleep Mode: SHDN\ = 0V, CS\ = 5V			1		µA
Power Dissipation	PDIS		1		150	240	mW
			2				
			3				
Power Dissipation	PDIS	Nap Mode: SHDN\ = 0V, CS\ = 0V	1		7.5	12	mW
			2				
			3				
Power Dissipation	PDIS	Sleep Mode: SHDN\ = 0V, CS\ = 5V			1.2		mW

Product Specification

Aeroflex RAD, Inc. Proprietary
UNCONTROLLED COPY

SIZE
A

CAGE CODE
3KTA5

REVISION LEVEL
F

DRAWING NUMBER
RAD-1419ADC-01

SHEET
6 of 19

TABLE II. Electrical performance characteristics (continued)

TIMING CHARACTERISTICS (* denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C.) Note 5

PARAMETER	SYM	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
Maximum Sampling Frequency	fSAMPLE(MAX)	*	9	800			kHz
			10				
			11				
Conversion Time	tCONV	Note 9/ *	9		950	1150	ns
			10				
			11				
Acquisition Time	tACQ	Note 9/ *	9		90	300	ns
			10				
			11				
Acquisition + Conversion Time	tACQ + CONV	Note 9/ *	9		1040	1250	ns
			10				
			11				
CS\ to RD\ Setup Time	t1	Note 9/ *		0			ns
CS\ to CONVST\ Setup Time	t2	Note 9/ *		40			ns
CS\ to SHDN\ Setup Time	t3	Note 9/		40			ns
SHDN\ to CONVST\ Wake-up Time	t4	Note 10/			400		ns
CONVST\ Low Time	t5	Notes 9/,11/ *	9	40			ns
			10				
			11				
CONVST\ to BUSY\ Delay	t6	CL = 25pF	9		20		ns
CONVST\ to BUSY\ Delay	t6	CL = 25pF, Note 9/	9			50	ns
			10				
			11				
Data Ready Before BUSY\	t7		9	20	50		ns
Data Ready Before BUSY\	t7	Note 9/	9	15			ns
			10				
			11				
Delay Between Conversions	t8	Note 9/ *	9	40			ns
			10				
			11				
Wait Time RD\ After BUSY\	t9	Note 9/ *		-5			ns
Data Access Time After RD\	t10	CL = 25pF	9		15	25	ns
Data Access Time After RD\	t10	CL = 25pF, Note 9/	9			35	ns
			10				
			11				
Data Access Time After RD\	t10	CL = 100pF, Note 9/	9		20	35	ns
Data Access Time After RD\	t10	CL = 100pF, Note 9/	9			50	ns
			10				
			11				

Product Specification

Aeroflex RAD, Inc. Proprietary
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SIZE
A

CAGE CODE
 3KTA5

REVISION LEVEL
 F

DRAWING NUMBER
RAD-1419ADC-01

SHEET
 7 of 19

TABLE II. Electrical performance characteristics (continued)

TIMING CHARACTERISTICS (* denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C.) Note 5

Bus Relinquish Time	t11	Note 9/	9		10	20	ns
Bus Relinquish Time	t11		9			35	
			10				
			11				
RD\ Low Time	t12	Note 9/ *	9	t10			ns
			10				
			11				
CONVST\ High Time	t13	Note 9/ *	9	40			ns
			10				
			11				

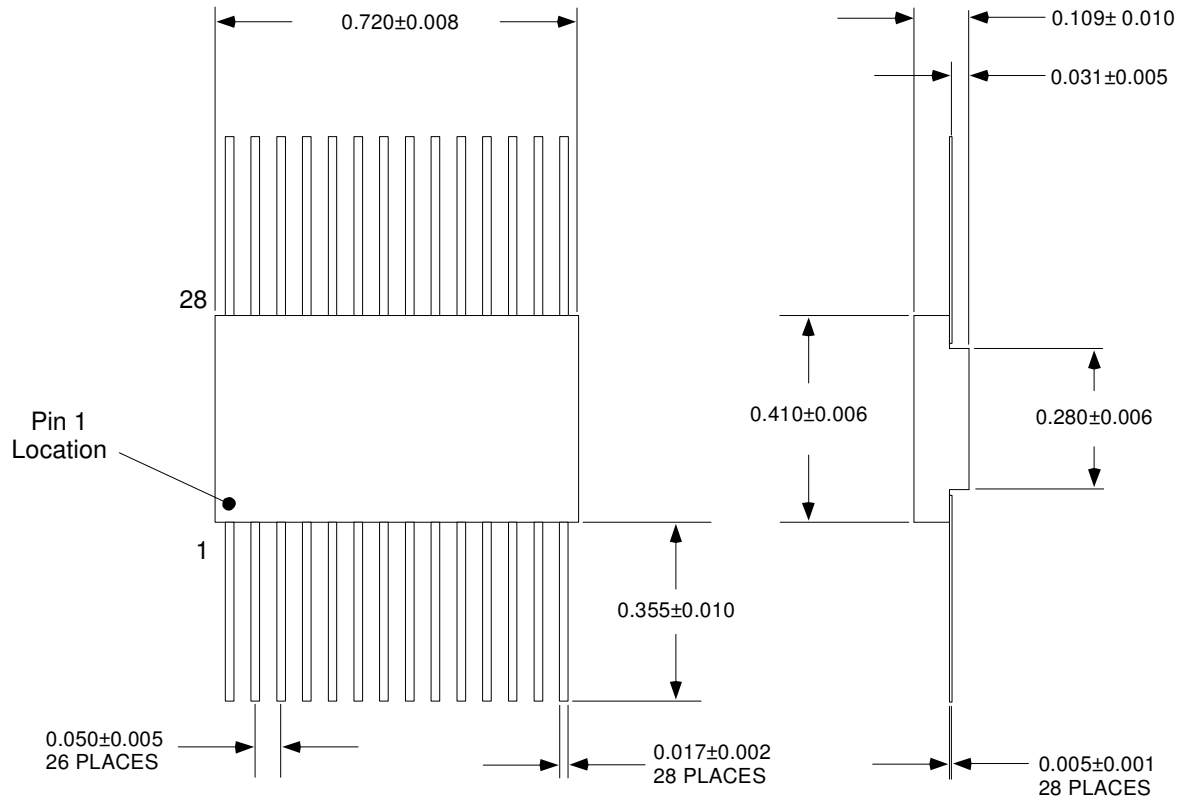
NOTES:

Parameters listed only as “Typical” are not tested in production.

- 1/ Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
- 2/ All voltage values are with respect to ground with DGND and AGND wired together unless otherwise noted.
- 3/ When these pin voltages are taken below VSS or above VDD, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below VSS or above VDD without latch up.
- 4/ When these pin voltages are taken below VSS, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below VSS without latch up. These pins are not clamped to VDD.
- 5/ VDD = 5V, VSS = -5V, fSAMPLE = 800kHz, tr = tf = 5ns unless otherwise specified.
- 6/ Linearity, offset and full-scale specifications apply for a single ended +AIN input with - AIN grounded.
- 7/ Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.
- 8/ Bipolar offset is the offset voltage measured from -0.5LSB when the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11.
- 9/ Guaranteed by design or characterization, not subject to test in production.
- 10/ Recommended operating conditions.
- 11/ The falling edge of CONVST\ starts a conversion. If CONVST\ returns high at a critical point during the conversion it can create small errors. For best performance ensure that CONVST\ returns high either within 650ns after the start of the conversion
- 12/ VIH and VIL will be guaranteed by testing VOH and VOL at the appropriate levels.

Product Specification	SIZE A	CAGE CODE 3KTA5	DRAWING NUMBER RAD-1419ADC-01
	Aeroflex RAD, Inc. Proprietary UNCONTROLLED COPY	REVISION LEVEL F	SHEET 8 of 19

FIGURE 1. Case outline.



All dimensions are in inches

FIGURE 2. Terminal connections.

Function	Pin	Function	Pin
+AIN	1	AVDD	28
-AIN	2	DVDD	27
REF	3	VSS	26
REFcomp	4	BUSY\	25
AGND	5	CS\	24
D13	6	CONVST\	23
D12	7	RD\	22
D11	8	SHDN\	21
D10	9	D0	20
D9	10	D1	19
D8	11	D2	18
D7	12	D3	17
D6	13	D4	16
DGND	14	D5	15

Product Specification

Aeroflex RAD, Inc. Proprietary
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SIZE
A

CAGE CODE
3KTA5

REVISION LEVEL
F

DRAWING NUMBER
RAD-1419ADC-01

SHEET
9 of 19

Order Shown According to Top View

PIN FUNCTIONS

+AIN (Pin 1): $\pm 2.5V$ Positive Analog Input.

-AIN (Pin 2): $\pm 2.5V$ Negative Analog Input.

VREF (Pin 3): 2.5V Reference Output. Bypass to AGND with $1\mu F$.

REFCOMP (Pin 4): 4.06V Reference Output. Bypass to AGND with $10\mu F$ tantalum in parallel with $0.1\mu F$ or $10\mu F$ ceramic.

AGND (Pin 5): Analog Ground.

D13 to D6 (Pins 6 to 13): Three-State Data Outputs. The output format is 2's complement.

DGND (Pin 14): Digital Ground for Internal Logic. Tie to AGND.

D5 to D0 (Pins 15 to 20): Three-State Data Outputs. The output format is 2's complement.

SHDN\ (Pin 21): Power Shutdown Input. Low selects shutdown. Shutdown mode selected by CS\, CS\ = 0 for nap mode and CS\ = 1 for sleep mode.

RD\ (Pin 22): Read Input. This enables the output drivers when CS\ is low.

CONVST\ (Pin 23): Conversion Start Signal. This active low signal starts a conversion on its falling edge.

CS\ (Pin 24): Chip Select. The input must be low for the ADC to recognize CONVST\ and RD\ inputs. CS\ also sets the shutdown mode when SHDN\ goes low. CS\ and SHDN\ low select the quick wake-up nap mode. CS\ high and SHDN\ low select sleep mode.

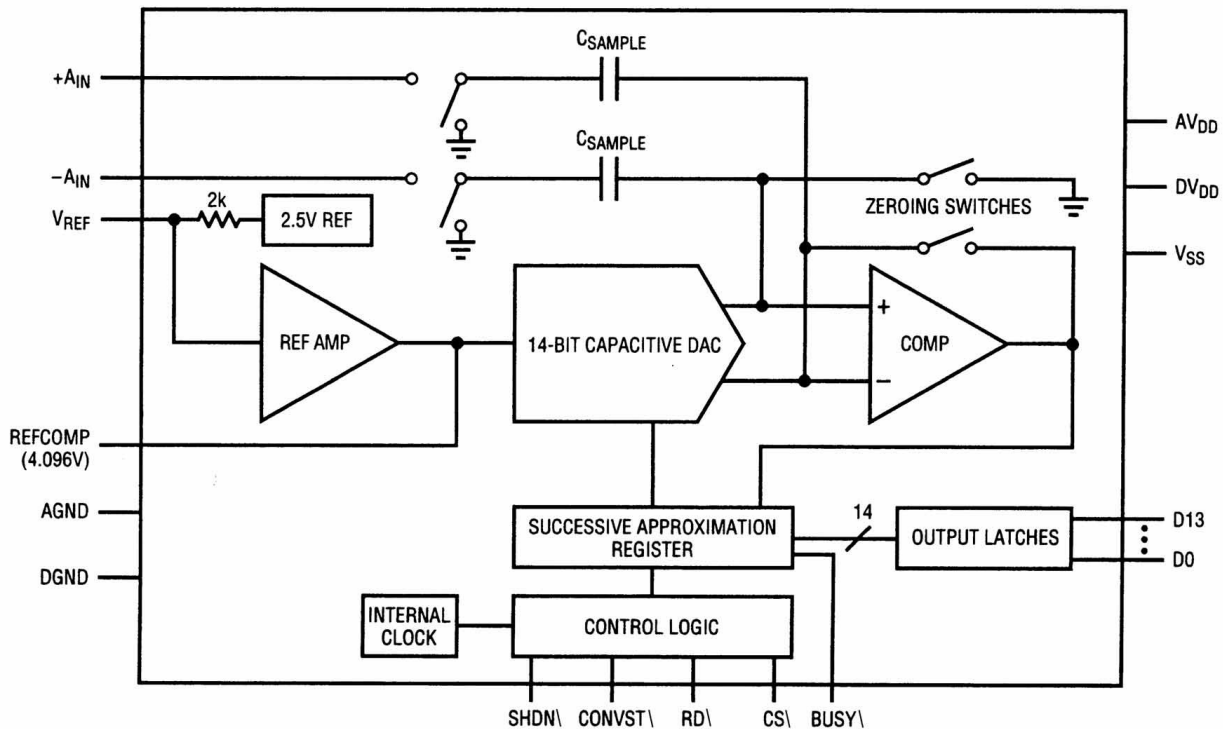
BUSY\ (Pin 25): The BUSY\ output shows the converter status. It is low when a conversion is in progress. Data valid on the rising edge of BUSY\.

V_{SS} (Pin 26): -5V Negative Supply. Bypass to AGND with $10\mu F$ tantalum in parallel with $0.1\mu F$ or $10\mu F$ ceramic.

DV_{DD} (Pin 27): 5V Positive Supply. Short to Pin 28.

AV_{DD} (Pin 28): 5V Positive Supply. Bypass to AGND with $10\mu F$ tantalum in parallel with $0.1\mu F$ or $10\mu F$ ceramic.

FIGURE 3. Block diagram.



Product Specification

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SIZE
A

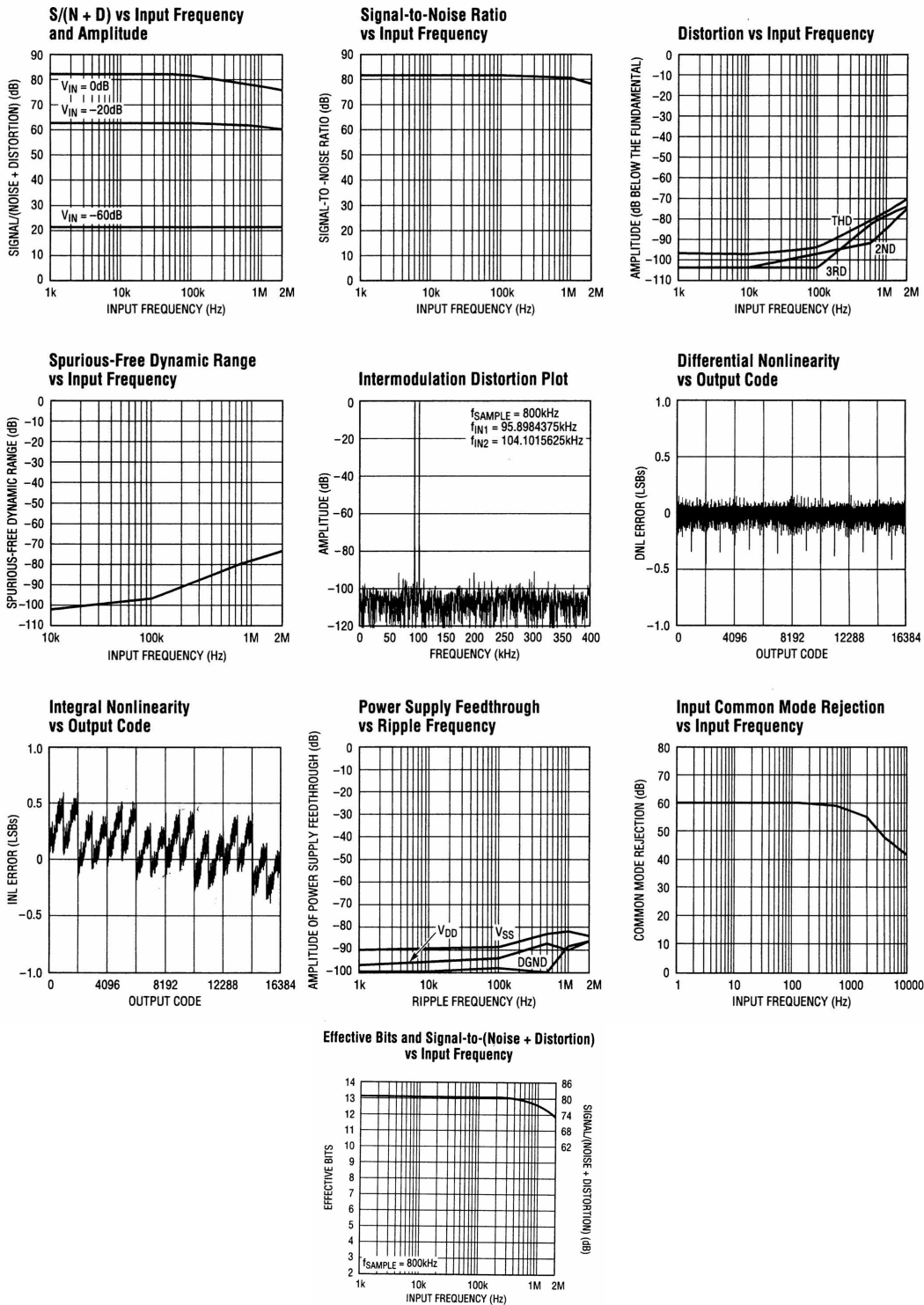
CAGE CODE
3KTA5

REVISION LEVEL
F

DRAWING NUMBER
RAD-1419ADC-01

SHEET
10 of 19

FIGURE 4. Typical Performance Characteristics



Product Specification

Aeroflex RAD, Inc. Proprietary
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SIZE
A

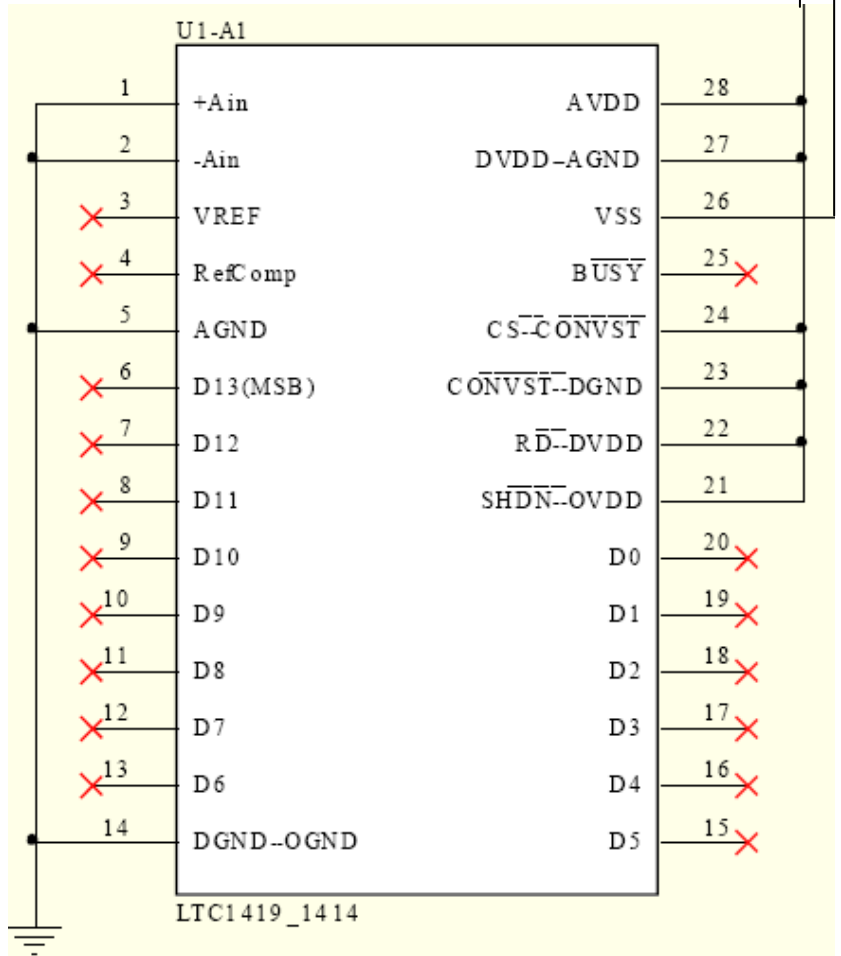
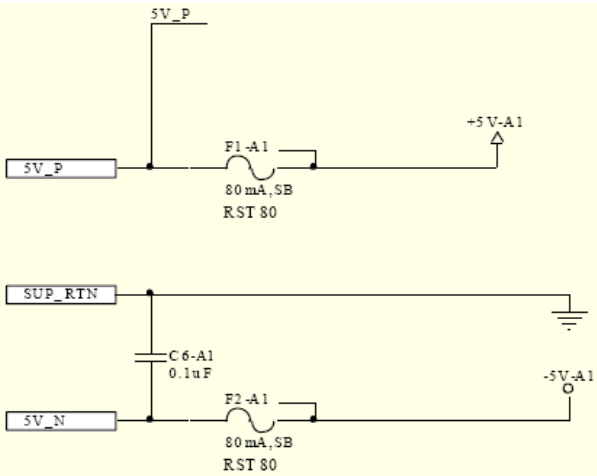
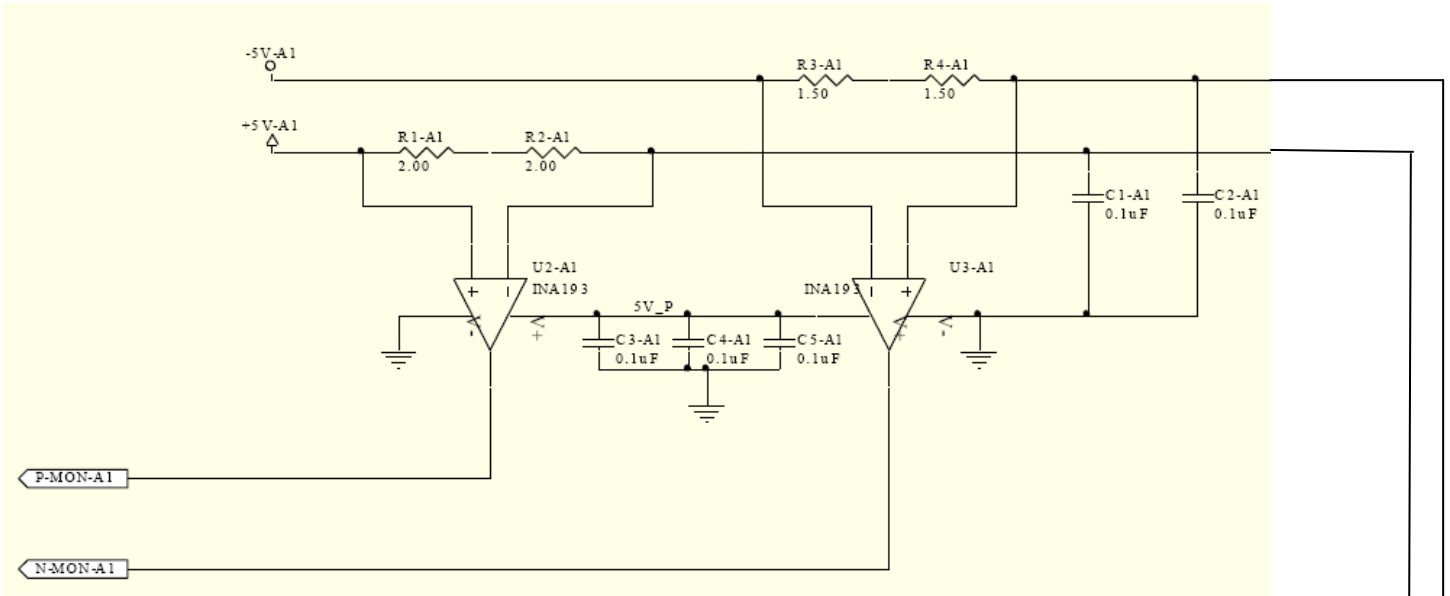
CAGE CODE
 3KTA5

DRAWING NUMBER
RAD-1419ADC-01

REVISION LEVEL
 F

SHEET
 11 of 19

FIGURE 5. Burn-in / Lifetest Schematic



Product Specification

Aeroflex RAD, Inc. Proprietary
UNCONTROLLED COPY

SIZE
A

CAGE CODE
 3KTA5

DRAWING NUMBER
RAD-1419ADC-01

REVISION LEVEL
 F

SHEET
 12 of 19

FIGURE 6. Radiation Bias Connection Table

FUNCTION	PIN NUMBER	BIAS CONNECTIONS DURING IRRADIATION
+A _{IN}	1	+2.5V, 1000pF Ceramic to -A _{IN}
-A _{IN}	2	GND
V _{REF}	3	10μF Ceramic to GND
REFCOMP	4	10μF Ceramic to GND
AGND	5	GND
D13 (MSB)	6	Open
D12	7	Open
D11	8	Open
D10	9	Open
D9	10	Open
D8	11	Open
D7	12	Open
D6	13	Open
DGND	14	GND
D5	15	Open
D4	16	Open
D3	17	Open
D2	18	Open
D1	19	Open
D0	20	Open
SHDN/	21	+5.5 V ± 0.15 V
RD/	22	GND
CONVST/	23	500 kHz Square Wave @ 5 % Duty Cycle
CS/	24	GND
BUSY/	25	Open
V _{SS}	26	-5.5 V ± 0.15 V, 10μF Ceramic to GND
DV _{DD}	27	Pin 28
AV _{DD}	28	+5.5 V ± 0.15 V, 10μF Ceramic to GND

Product Specification

Aeroflex RAD, Inc. Proprietary
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SIZE
A

CAGE CODE
 3KTA5

DRAWING NUMBER
RAD-1419ADC-01

REVISION LEVEL
 F

SHEET
 13 of 19

4. VERIFICATION

- 4.1 Sampling and inspection. For HI-REL device, sampling and inspection procedures shall be in accordance with the tables in this section unless otherwise specified in customer documentation.
- 4.2 Screening. For HI-REL device, screening shall be in accordance with Table III, test methods form MIL-STD-883, and shall be conducted on all devices prior to qualification and technology conformance inspection.
 - 4.2.1 Scanning Electron Microscope (SEM) Inspection. SEM inspection, when required, shall be performed on a random sampling of die from one wafer in each wafer lot. SEM inspection shall be per Method 2018, Table II of MIL-STD-883.
 - 4.2.2 Internal Visual Inspection. Internal visual inspection shall be performed in accordance with Method 2010 of MIL-STD-883 as applicable.
 - 4.2.3 Interim and Final Electrical Parameters. Interim and final electrical test parameters shall be as specified in Table II herein. Variables data for each test of each device when specified shall be recorded and traceability shall be maintained by individual device serial number and by lot number.
 - 4.2.4 Burn-In. Burn-in shall be in accordance with Method 1015 of MIL-STD-883, and Table II herein. The burn-in circuit(s) as specified on Figure 5 herein.
 - 4.2.5 Percent Defective Allowable (PDA). The PDA, when required shall be calculated on those devices whose measured characteristics after burn-in exceed the specified delta limits or exceed the electrical parameter limits specified in Table II. The verified failures divided by the total number of die in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA. The PDA shall be three (3) percent or 1 part whichever is greater, based on the exact number of devices submitted to each burn-in.

TABLE III: Screening

SCREEN	METHOD	CONDITION	NOTES
Non-destructive bond pull	2023		
Internal visual	2010	Condition A	
Serialization	--	--	<u>1/</u>
Temperature cycling	1010	Condition C, 10 cycles -65 C to +150 C	
Constant Acceleration	2001	Condition E, Y1 Axis	
PIND	2020	Condition A	
Radiography	2018	Y1 Axis	<u>2/</u>
Pre-burn in electrical test	--	25 Deg C , See Tables II & IV	
Static burn-In	2015	Condition B, 240 hrs at 125C	
Interim, post burn In electrical	--	25 Deg C , See Tables II & IV	
PDA- calculation	--	--	
Delta calculation	--	--	
Final electrical test, room	--	25 Deg C , See Tables II & IV	
Final electrical test, hot	--	125 Deg C , See Tables II & IV	
Final electrical test, cold	--	-55 Deg C , See Tables II & IV	
Final Electrical			
Seal test	1014	Cond B1, B2	
Post Seal electrical test (optional)		25 Deg C , See Tables II & IV	
External visual	2009	--	

1/ May be performed anytime before pre-burn in electrical test.

2/ May be performed anytime after serialization.

Product Specification Aeroflex RAD, Inc. Proprietary UNCONTROLLED COPY	SIZE A	CAGE CODE 3KTA5	DRAWING NUMBER RAD-1419ADC-01
		REVISION LEVEL F	SHEET 14 of 19

4.3 Qualification and conformance inspection for Hi-Rel device. Unless otherwise specified, qualification and conformance inspection shall be in accordance with Tables IV, V and VI below.

4.3.1 Group A inspection.

4.3.1.1 Tests shall be as specified in Table IV herein. Group A testing shall be accordance with MIL-STD-883, Method 5005, Table I and footnotes with the exception that the sample size shall be 25 parts and 0 failures allowed. (NOTE: Post burn-in electrical reject devices from the same inspection lot may be used for all Groups B and D subgroups when end-point measurements are not required. The sample size for Group A testing may be reduced when these units are used, however, the minimum Group A sample size is 20 devices and 0 failures allowed).

TABLE IV. Electrical test requirements

Test Requirements	Subgroups
Pre Burn-in electrical parameters	1,4,9
Interim electrical parameters	1,4,9
Final electrical test parameters	1,2,3,4 ,9,10,11
Post Seal electrical test parameters	1
Group A electrical test parameters	1,2,3,4,9,10,11
Group B electrical test parameters	1,4,9
Group C electrical test parameters	1,4,9
Group D electrical test parameters	1,4,9

Subgroups	Definitions
1	Static Characteristics 25°C
2	Static Characteristics 125°C
3	Static Characteristics -55°C
4	Dynamic Characteristics 25°C
5	Dynamic Characteristics 125°C
6	Dynamic Characteristics -55°C
9	Switching Characteristics 25°C
10	Switching Characteristics 125°C
11	Switching Characteristics -55°C

Product Specification

Aeroflex RAD, Inc. Proprietary
UNCONTROLLED COPY

SIZE
A

CAGE CODE
3KTA5

DRAWING NUMBER
RAD-1419ADC-01

REVISION LEVEL
F

SHEET
 15 of 19

4.3.2 Group B inspection. Group B inspection shall be performed as follows in Table V

TABLE V: Group B Conformance Inspection

SUBGROUP & TEST <u>1/ 2/ 10/</u>	MIL-STD-883 METHOD	CONDITION	SAMPLE SIZE (ACC NO.) <u>3/</u>
<u>Subgroup 1</u>			
a) Physical dimensions	2016		2(0)
b) Internal water-vapor content	1018	5000ppm max water @ 100C	3(0) or 5(1)
<u>Subgroup 2</u>			
a) Resistance to solvents	2015		3(0)
b) Internal visual	2013/2014		2(0)
c) Bond strength <u>4/</u>	2011		22(0)
d) Die shear	2019		3(0)
<u>Subgroup 3</u>			
a) Solderability <u>8/</u>	2003		22(0)
<u>Subgroup 4</u>			
a) Lead integrity <u>9/</u>	2004		45(0)
b) Seal <u>6/</u> (fine and gross)	1014	Condition B1, B2	2(0)
c) Lid torque <u>5/</u>	2024		2(0)
<u>Subgroup 5 7/</u>			
a) Electrical parameters			
b) Steady state life	1005	1000 hrs @125 °C	45(0)
c) Electrical parameters			
<u>Subgroup 6 7/</u>			
a) Electrical parameters			
b) Temperature cycling	1010	Condition C 100 cycles -65°C to +150°C	
c) Constant acceleration,	2001	Condition E, Y1 Only	15(0)
d) Seal (fine and gross)	1014	Condition B1, B2	
e) Electrical parameters			

1/ Post burn-in electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required. Sequence of tests may be altered at supplier's option.

2/ Delta failures may be used for Subgroups 1 through 4.

3/ Quantities stated represent minimum quantities. If larger sample sizes are used, the reject criteria shall not change, unless otherwise specified.

4/ Pull 22 wires from 2 devices.

5/ Lid torque test shall apply only to glass-frit sealed packages.

6/ Test Conditions D and E prohibited.

7/ Samples shall be randomly selected from the lot after successful completion of Group A. Group A data may be used for pre-electrical test data.

8/ Perform solderability testing on 22 leads from 2 devices.

9/ Perform lead integrity testing on 22 leads from 2 devices.

10/ Unless otherwise specified, all electrical test conditions and end points shall be per customer SCD or product specification.

Product Specification

Aeroflex RAD, Inc. Proprietary
UNCONTROLLED COPY

SIZE
A

CAGE CODE
3KTA5

DRAWING NUMBER
RAD-1419ADC-01

REVISION LEVEL
F

SHEET
16 of 19

4.3.3 Group D inspection. Group D qualification inspection shall be as follows in Table VI.

TABLE VI: Group D Qualification Inspection

SUBGROUP & TEST <u>1/ 2/ 4/ 9/</u>	MIL-STD-883 METHOD	CONDITION	SAMPLE SIZE (ACC NO.) <u>3/</u>
<u>Subgroup 3</u>			
a) Thermal shock,	1011	Condition B 15 Cycles, -55°C to 125°C	15(0)
b) Temperature cycling	1010	Condition C 100 Cycles, -65°C to 150°C	
c) Moisture resistance	1004		
d) Visual examination	1004/1010		
e) Seal <u>4/</u> (fine and gross)	1014	B1, B2	
f) End point electrical parameters <u>7/</u>	--		
<u>Subgroup 4 5/</u>			
a) Mechanical shock	2002	Condition B 1.5Kg (peak) 0.5 ms pulse	15(0)
b) Vibration, variable frequency	2007	Condition A 20g peak	
c) Constant acceleration	2001	Condition E Y1 Orientation	
d) Seal <u>4/</u> (fine and gross)	1014	B1, B2	
e) Visual examination			
f) End-point electrical parameters			
<u>Subgroup 5 1/</u>			
a) Salt atmosphere	1009	Condition A	15(0)
b) Visual examination			
c) Seal (fine and gross)	1014	B1, B2	
<u>Subgroup 7</u>			
a) Adhesion of lead finish <u>6/ 8/</u>	2025		22(0)

- 1/ Post burn-in electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required. Sequence of tests may be altered at supplier's option.
- 2/ Unless otherwise specified, all electrical test conditions and end points shall be per customer SCD or product specification.
- 3/ Quantities stated represent minimum quantities. If larger sample sizes are used, the reject criteria shall not change, unless otherwise specified.
- 4/ Test conditions D and E prohibited.
- 5/ Subgroup 3 samples may be used for Subgroup 4.
- 6/ Samples may be taken from Group B, Subgroup 6.

Product Specification

Aeroflex RAD, Inc. Proprietary
UNCONTROLLED COPY

SIZE
A

CAGE CODE
3KTA5

REVISION LEVEL
F

DRAWING NUMBER
RAD-1419ADC-01

SHEET
17 of 19

7/ At the supplier's option, end-point electrical parameters may be performed after moisture resistance and prior to Seal test.

8/ Perform Adhesion of lead finish on 22 leads from 2 devices.

5. Radiation Characterization. Radiation specifications for TID, ELDRS, SEU, Neutron Displacement Damage and Prompt Dose are listed below.

5.1 Total Ionizing Dose (TID) – Post-rad performance specifications are as shown in Table VII. A detailed TID characterization report is available.

5.2 Enhanced Low Dose Rate Sensitivity (ELDRS) – Immune by technology.

5.3 Single Event Latch-up (SEU) – No latch-up exhibited at any LET of 55MeV-cm²/mg or lower at a case temperature of 85°C. A detailed SEL characterization report is available.

5.4 Neutron Displacement Damage – Immune by technology.

5.5 Prompt Dose Latch Up – Not characterized.

Table VII. Post Radiation Performance

TEST	SYM	TEST CONDITION	0KRAD(SI)		10KRAD(SI)		30KRAD(SI)		50KRAD(SI)		100KRAD(SI)		Units
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Integral Linearity Error	INL		-2	2	-2	2	-2	2	-3	3	-5	5	LSB
Differential Linearity Error	DNL		-1	1	-1	1	-1	1	-1	1	-3	3	LSB
Offset Error			-20	20	-20	20	-20	20	-30	20	-40	20	LSB
Analog Input Leakage Current	IIN	CS\ = HIGH	-1	1	-1	1	-1	1	-1	1	-1	1	µA
Signal-to (Noise + Distortion) Ratio	S(N + D)	100kHz Input Signal	78		78		78		75		70		dB
Total Harmonic Distortion	THD	100kHz Input Signal, First 5 Harmonics		-86		-86		-86		-84		-82	dB
Spurious Free Dynamic Range	SFDR	100kHz Input Signal	86		86		86		86		86		dB
Output Voltage	VREF	IOUT = 0	2.48	2.52	2.48	2.52	2.48	2.52	2.48	2.52	2.48	2.52	V
High Level Input Voltage	VIH	VDD = 5.25V Note 12	2.4		2.4		2.4		2.4		2.4		V
Digital Input Current	IIN	VIN = 0V to VDD	-10	10	-10	10	-10	10	-10	10	-10	10	µA
Low Level Input Voltage	VIL	VDD = 4.75V Note 12		0.8		0.8		0.8		0.8		0.8	V
High Level Output Voltage	VOH	VDD = 4.75V IO = -200µA	4		4		4		4		4		V
Low Level Output Voltage	VOL	VDD = 4.75V IO = 1.6mA		0.4		0.4		0.4		0.4		0.4	V
High-Z Output Leakage D13 to D0	IOZ	VOUT = 0V to VDD, CS\ High	-10	10	-10	10	-10	10	-10	10	-10	10	µA

Product Specification

Aeroflex RAD, Inc. Proprietary
UNCONTROLLED COPY

SIZE
A

CAGE CODE
3KTA5

DRAWING NUMBER
RAD-1419ADC-01

REVISION LEVEL
F

SHEET
18 of 19

6. PACKAGING

6.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

7. NOTES

7.1 Substitutability. Device class Q devices will replace device class M devices.

7.2 Configuration control of this drawing. All proposed changes will be coordinated with the users of record.

7.3 Record of users. Military and industrial users should inform Aeroflex RAD, Inc. when a system application requires configuration control.

7.4 Comments. Comments on this drawing should be directed to Aeroflex RAD, Inc. (719)-531-0800

7.5 Updates. This document is not controlled for up-dates. Please contact Aeroflex RAD to check the latest revision.

Product Specification Aeroflex RAD, Inc. Proprietary UNCONTROLLED COPY	SIZE A	CAGE CODE 3KTA5	DRAWING NUMBER RAD-1419ADC-01
		REVISION LEVEL F	SHEET 19 of 19